

CLAIMS

- 1 1. A low voltage differential amplifier architecture with differential input and output
2 signals, comprising,
3 a first stage comprising a first set of common source connected first identical
4 NMOS transistors and parallel first identical PMOS transistors with their respective gates
5 connected to the differential input signal,
6 a first current source connected to the sources of the first NMOS transistors and a
7 second current source connected to the sources of the first PMOS transistors,
8 the drains of the first NMOS transistors are connected to sources of a set of sec-
9 ond identical PMOS transistors,
10 the drains of the first PMOS transistors are connected to sources of a set of second
11 identical NMOS transistors, wherein the second identical PMOS and the second identical
12 NMOS transistors are in a second stage, wherein each of the second identical NMOS
13 transistors and each of the second identical PMOS transistors are symmetrical to each
14 other, and
15 wherein the drain of one of the second PMOS transistors is connected to the drain
16 of one of the set of second identical NMOS transistors, thereby forming a first current
17 path, and
18 wherein the drain of the other of the second PMOS transistors is connected to the
19 drain of the other of the set of second identical NMOS transistors, thereby forming a sec-
20 ond current path,
21 wherein the voltage signal between the commonly connected drains defines an
22 intermediate differential output signal,
23 a first biasing tree including a first tree PMOS transistor and a first tree NMOS
24 transistor, with drains and gates connected to each other, the source of the first tree
25 PMOS connected to the source of the source of the PMOS in the first current path,
26 wherein the first tree PMOS and the PMOS in the first current path for a first current mir-
27 ror, and the source of the first tree NMOS connected to the source of the NMOS in the

28 first current path, wherein the first tree NMOS and the NMOS in the first current path
29 form a second current mirror,
30 a second biasing tree including a second tree PMOS transistor and a second tree
31 NMOS transistor, with drains and gates connected to each other, the source of the second
32 tree PMOS connected to the source of the source of the PMOS in the second current path,
33 wherein the second tree PMOS and the PMOS in the second current path form a third
34 current mirror, and the source of the second tree NMOS connected to the source of the
35 NMOS in the second current path, wherein the second tree NMOS and the NMOS in the
36 second current path form a fourth current mirror,
37 wherein all the gates of the PMOS and NMOS transistors in the first and the sec-
38 ond current paths and in the first and second biasing trees all are connected together,
39 a third current source connected to the source of the PMOS transistors in the first
40 current path,
41 a fourth current source connected to the source of the PMOS transistors in the first
42 current path, wherein the third current source and the fourth current source are equal to
43 each other and each is of a higher value than the second current source,
44 a fifth current source connected to the sources of the NMOS transistors in the sec-
45 ond current path,
46 a sixth current source connected to the sources of the NMOS transistors in the
47 second current path, wherein the fifth current source and the sixth current source are
48 equal to each other and each is of a higher value than the first current source,
49 a third differential stage with a differential input connected to the intermediate
50 differential output, and the third differential stage providing a differential output.

1 2. The circuit as defined in claim 1 wherein the arrangements of the corresponding
2 sets of transistors and current sources are symmetrical with respect to each other and
3 further comprising the circuit is laid out such that the current paths on either signal path
4 side of the differential topology are identical to each other and further wherein imped-
5 ances are equal to each other traveling on either signal path side of the differential circuit.

1 3. The circuit as defined in claim 1 further comprising two buffer inverters each ac-
2 cepting one of the differential output signals and each providing an output suitable for
3 driving a number of loads.

1 4. A low voltage differential amplifier architecture with differential input and output
2 signals, comprising,
3 parallel complementary common source first NMOS and first PMOS transistor
4 pairs with their gates accepting the differential input signal,
5 complementary current sources feeding the source of the first NMOS and first
6 PMOS transistor pairs, the complementary current sources and first NMOS and first
7 PMOS transistor pairs forming a differential input stage, and
8 a second PMOS pair arranged for accepting the drains of the first NMOS pair,
9 a second NMOS pair arranged for accepting the drains of the first PMOS pair,
10 wherein the drains of the second NMOS pair are connected to the corresponding drains of
11 the second PMOS pair, wherein the second NMOS and PMOS pairs form a folded
12 cascode differential output stage,
13 a pair of stacked PMOS and NMOS transistor structures with drains connected
14 together, thereby providing complementary biasing current mirroring stacks for the out-
15 put cascode second NMOS and second PMOS pairs, and further where the all the gates of
16 the second PMOS and second NMOS and stacked PMOS and stacked NMOS transistors
17 are all connect together, and
18 wherein one of the stacked PMOS sources and the source of one of the second
19 PMOS pair are connected together to a first node, and where the second of the stacked
20 PMOS sources and the source of the other of the second PMOS pair are connected to-
21 gether to a second node, and one of the stacked NMOS sources and the source of one of
22 the second NMOS pair are connected together to a third node, and where the second of
23 the stacked NMOS sources and the source of the other of the second NMOS pair are con-
24 nected together to a fourth node,

25 four complementary current sources, one connected to the first node, a second
26 connected to the second node, a third connected to the third node and the fourth con-
27 nected to the fourth node, and

28 a third differential stage with a differential input connected to the intermediate
29 differential output, and the third differential stage providing a differential output.

1 5. The low voltage differential amplifier of claim 4 wherein the first and second cur-
2 rent sources are equal to each other and their source complementary current sources are
3 each equal to each other and where each is at least greater than one half the value of the
4 first or second current source.

1 6. A low voltage differential amplifier of the type having a first stage including a
2 PMOS and NMOS differential transistor pairs and first current sources that are distrib-
3 uted between a low and a high voltage source, the pairs arranged to handle common
4 mode input signals from the low to the high voltage, and wherein the output of the first
5 stage is a differential current that is input to a second stage, wherein the second stage is of
6 the type including parallel paths of first stacked PMOS and NMOS transistors distributed
7 between the low and high voltage sources, and parallel legs of second stacked PMOS and
8 NMOS transistors, each of the second stacked transistors providing a bias for one of the
9 first stacked legs, and wherein the gates of the first and second stacked transistors are
10 connected together, and, furthermore, including four current sources, two between the
11 stacked legs and the high voltage source and two between the low voltage source and the
12 stacked legs, wherein the four current sources are each equal to each other and each is of
13 a value higher than one half that of each of the first current sources.

1 7. The differential amplifier of claim 6 further comprising an output differential
2 voltage from the common drains of the first stacked PMOS and NMOS legs, and a third
3 differential amplifier that accepts the differential outputs and provides differential voltage
4 output wherein each of the two differential signals are arranged to traverse from the low
5 to the high voltage sources.